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| 10/016,693 | 10/30/2001 | Michael D. Lammert | 12-1233 | 2474 |

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| EXAMINER | |
|---|---|
| MALDONADO, JULIO J | |
| **ART UNIT** | **PAPER NUMBER** |
| 2823 | |

DATE MAILED: 07/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Offic Action Summary | Application No. 10/016,693 | Applicant(s) LAMMERT, MICHAEL D. | |
|---|---|---|---|
| | Examiner Julio J. Maldonado | Art Unit 2823 | |

*-- The MAILING DATE of this communication appears on th cover sheet with the correspondenc address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 13 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Ping (U.S. 5,616,519).

Ping (Figs.1-9) in a related method to form metal interconnect structures teach the steps of providing a substrate layer (1); forming a lower level layer ~~of~~ on said substrate (1) selected from one or more of the group consisting of dielectric, metal and a circuit device; forming a bottom metal layer (9) on said lower level layer (2-6); forming one or more pillars (11) from a photoresist on said lower metal layer (9); coating said one or more pillars (11) with a silicon based polymer (13); curing said polymer (13); etching back said polymer (13) to expose one or more pillars (11); removing said one or more photoresist pillars (11) to form vias (15); and forming a metal layer (17) to contact said bottom metal layer (9) on top of said polymer coating (13) (column 2, line 65 – column 5, line 27).

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 4, 5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kano (U.S. 5,380,679) in view of Lin (U.S. 5,929,525).

In reference to claims 1 and 7, Kano (Figs.2A-2G) in a related method to form interconnect structures teaches providing a substrate layer (1); forming a lower level layer (2) on said substrate layer, selected from one or more of the group consisting of dielectric, metal and circuit devices; forming a seed layer (3) on top of said lower level layer; forming a lower metal layer (5) on said seed layer (4); forming, one or more pillars (8) from a photoresist having top surfaces on said lower metal layer (5), defining photoresist pillars (8); plating said photoresist pillars (8) defining plated pillars (10); removing the seed layer (3) not under the lower level layer; forming a dielectric layer (7); and forming a metal layer (12, 13) over said dielectric layer (11), the metal layer (12, 13) contacting an exposed top surface of said plated pillars (10) (column 4, line 17 – column 5, line 57).

Kano fails to teach coating said one or more plated pillars and said seed layer with a low dielectric polymer; curing said polymer; exposing said top surfaces of said dilated pillars; and forming a metal layer to contact said exposed top surfaces of said plated pillars. However, Lin (Figs.1-9) in a related method to form an interconnect

structure teaches the steps of providing a substrate layer (1); forming a lower level layer on said substrate, selected from one or more of the group consisting of dielectric, metal and circuit devices; forming a lower metal layer (9) on said devices (2-7); forming one or metal pillars (12) having top surfaces on said lower metal layer (9); coating said one or more metal pillars with a silicon based dielectric polymer (14); curing said polymer (14); exposing said top surfaces of said metal pillars (12); and forming a metal layer (16) to contact said exposed top surfaces of said metal pillars (11) (column 2, line 50 – column 5, line 23). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kano and Lin to perform the dielectric coatings of Lin to arrive to the claimed invention, and furthermore to roughly planarize the existing topography by filling the spaces between metal pillars (column 4,lines 23 – 37).

In reference to claims 4 and 5, Lin teaches applying a dielectric layer (13) to said pillars (12) and said metal layer (9), wherein said dielectric layer comprises $SiO_2$ (column 2, line 50 – column 5, line 23).

6. Claims 2, 6, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kano ('679) in view of Lin ('525) as applied to claims 1, 4, 5 and 7 above, and further in view of the applicants admitted prior art.

Kano in combination with Lin substantially teach all aspect of the invention but fail to teach the steps of applying $Si_3N_4$; and coating the lower metal layer and the plated pillars with a material selected from the group including benzocyclobutene and polynorbornene. However, the prior art teaches the steps of applying $Si_3N_4$; and coating

the lower metal layer and the plated pillars with a material selected from the group including benzocyclobutene and polynorbornene (page 1, [0003] – page 3, [0008]). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use $Si_3N_4$, benzocyclobutene and polynorbornene as taught by the prior art in the interconnect formation method of Kano and Lin, since these are well-known materials used to form multilevel dielectric layers (page 1, [0003]).

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kano ('679) in view of Lin ('525) as applied to claims 1, 4, 5 and 7 above, and further in view of Sonego et al. (U.S. 6,239,042 B1).

The combination of Kano and Lin teach coating with a low-dielectric polymer, non planarizing polymer on the plated pillars and the lower metal layer (Lin, column 2, line 50 – column 5, line 23) but fail to teach forming a planarizing coating over said non-planarizing polymer. However, Sonego et al. teach forming a planarizing coating over a non-planarizing dielectric layer (column 5, lines 44-55). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the planarizing layer as taught by Sonego et al. in the interconnect formation method of Kano and Lin, since this would improve the planar connection of metal layers (column 1, lines 16 – 35).

8. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kano ('679) in view of Lin ('525) as applied to claims 1, 4, 5 and 7 above, and further in view of Furukawa et al. (U.S. 6,387,783 B1).

The combined method of Kano and Lin teach using a photoresist to form the plated pillars but fail to expressly teach using a photoresist with a re-entrant profile and using a negative i-line resist. However, Furukawa et al. (Figs.2A-2E) in a related method to pattern a metal layer teach using a photoresist (201) with a re-entrant profile and using a negative i-line resist (column 1, line 43 – 65). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use a photoresist as taught by Furukawa et al. in the interconnect formation method of Kano and Lin, since this would improve linewidth control in a multilayered stack (column 1, lines 25 – 33).

9. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kano ('679) in view of Lin ('525) and Furukawa et al. ('783 B1) as applied to claims 11 above, and further in view of Samoto (U.S. 5,583,063).

Kano in combination with Lin and Furukawa et al. teach using a negative photoresist to define a pattern (Furukawa et al., column 1, line 43 – 65) but fail to expressly teach using a $NH_3$ image reversal of a photoresist. However, Samoto (Figs.2A-2H) in a related to define a pattern for a semiconductor device teaches using a $NH_3$ image reversal of a photoresist (column 4, lines 18 – 36). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the photoresist of Samoto in the interconnect formation method of Kano, Lin and Furukawa et al., since this would allow the formation of defined small-sized patterns (column 2, lines 47-50).

10. Claims 14 and 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ping ('519) in view of Lin ('525).

Ping (Figs.1-9) in a related method to form metal interconnect structures teach the steps of providing a substrate layer (1); forming a lower level layer of on said substrate (1) selected from one or more of the group consisting of dielectric, metal and a circuit device; forming a bottom metal layer (9) on said lower level layer (2-6); forming one or more pillars (11) from a photoresist on said lower metal layer (9); coating said one or more pillars (11) with a silicon based polymer (13); curing said polymer (13); etching back said polymer (13) to expose one or more pillars (11); removing said one or more photoresist pillars (11) to form vias (15); and forming a metal layer (17) to contact said bottom metal layer (9) on top of said polymer coating (13) (column 2, line 65 – column 5, line 27).

Ping fails to teach forming a dielectric in top of said bottom metal layer and said lower level layer (2-6) before the coating step; and removing said dielectric layer form said bottom metal layer before a metal layer is formed on top of said polymer coating. However, Lin in a related method to form an interconnect structure teaches forming a dielectric (10) in top of a bottom metal layer (9) and said lower level layer (2-6) before a coating step; and removing said dielectric layer (10) form said bottom metal layer (9) before a metal layer is formed on top of a polymer coating (14) (column 2, line 50 – column 5, line 23). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide a dielectric layer as taught by Lin in

the interconnect formation method of Ping, since this would provide protection for the bottom metal layer (column 3, lines 52-55).

11. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ping ('519) in view of Kano ('Lin) as applied to claims 14 and 15 above, and further in view of the applicants admitted prior art.

Ping in combination with Lin substantially teach all aspect of the invention but fail to teach the applying a $Si_3N_4$ layer. However, the prior art teaches the steps of applying $Si_3N_4$ (page 1, [0003] – page 3, [0008]). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use $Si_3N_4$, as taught by the prior art in the method of Ping and Lin, since these are well-known materials used to form multilevel dielectric layers (page 1, [0003]).

12. Claims 17, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ping ('519) in view of the applicants admitted prior art.

Ping (Figs.1-9) in a related method to form metal interconnect structures teach the steps of providing a substrate layer (1); forming a lower level layer of on said substrate (1) selected from one or more of the group consisting of dielectric, metal and a circuit device; forming a bottom metal layer (9) on said lower level layer (2-6); forming one or more pillars (11) from a photoresist on said lower metal layer (9); coating said one or more pillars (11) with a silicon based polymer (13); curing said polymer (13); etching back said polymer (13) to expose one or more pillars (11); removing said one or more photoresist pillars (11) to form vias (15); and forming a metal layer (17) to contact

said bottom metal layer (9) on top of said polymer coating (13) (column 2, line 65 – column 5, line 27).

Ping fails to teach coating the lower metal layer and the photoresist pillars with a material selected from the group including benzocyclobutene and polynorbornene. However, the prior art teaches coating the lower metal layer and the plated pillars with a material selected from the group including benzocyclobutene and polynorbornene (page 1, [0003] – page 3, [0008]). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use benzocyclobutene and polynorbornene as taught by the prior art in the interconnect formation method of Ping, since these are well-known materials used to form multilevel dielectric layers (page 1, [0003]).

13. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ping ('519) in view of Sonego et al. ('042 B1).

Ping (Figs.1-9) in a related method to form metal interconnect structures teach the steps of providing a substrate layer (1); forming a lower level layer of on said substrate (1) selected from one or more of the group consisting of dielectric, metal and a circuit device; forming a bottom metal layer (9) on said lower level layer (2-6); forming one or more pillars (11) from a photoresist on said lower metal layer (9); coating said one or more pillars (11) with a silicon based polymer (13); curing said polymer (13); etching back said polymer (13) to expose one or more pillars (11); removing said one or more photoresist pillars (11) to form vias (15); and forming a metal layer (17) to contact

said bottom metal layer (9) on top of said polymer coating (13) (column 2, line 65 – column 5, line 27).

Also, Ping teaches coating with a low-dielectric polymer, non-planarizing polymer on the photoresist pillars and the lower metal layer but fails to teach forming a planarizing coating over said non-planarizing polymer. However, Sonego et al. teach forming a planarizing coating over a non-planarizing dielectric layer (column 5, lines 44-55). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the planarizing layer as taught by Sonego et al. in the interconnect formation method of Ping, since this would improve the planar connection of metal layers (column 1, lines 16 – 35).

14. Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ping ('519) in view of Furukawa et al. ('783 B1).

Ping (Figs.1-9) in a related method to form metal interconnect structures teach the steps of providing a substrate layer (1); forming a lower level layer of on said substrate (1) selected from one or more of the group consisting of dielectric, metal and a circuit device; forming a bottom metal layer (9) on said lower level layer (2-6); forming one or more pillars (11) from a photoresist on said lower metal layer (9); coating said one or more pillars (11) with a silicon based polymer (13); curing said polymer (13); etching back said polymer (13) to expose one or more pillars (11); removing said one or more photoresist pillars (11) to form vias (15); and forming a metal layer (17) to contact said bottom metal layer (9) on top of said polymer coating (13) (column 2, line 65 – column 5, line 27).

Ping also teaches using a photoresist to form the photoresist pillars but fails to expressly teach using a photoresist with a re-entrant profile and using a negative i-line resist. However, Furukawa et al. (Figs.2A-2E) in a related method to pattern a metal layer teach using a photoresist (201) with a re-entrant profile and using a negative i-line resist (column 1, line 43 – 65). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use a photoresist as taught by Furukawa et al. in the interconnect formation method of Ping, since this would improve linewidth control in a multilayered stack (column 1, lines 25 – 33).

15. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ping ('519) in view of Furukawa et al. ('783 B1) as applied to claims 11 above, and further in view of Samoto ('063).

Ping in combination with Furukawa et al. teach using a negative photoresist to define a pattern (Furukawa et al., column 1, line 43 – 65) but fail to expressly teach using a $NH_3$ image reversal of a photoresist. However, Samoto (Figs.2A-2H) in a related to define a pattern for a semiconductor device teaches using a $NH_3$ image reversal of a photoresist (column 4, lines 18 – 36). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the photoresist of Samoto in the interconnect formation method of Ping and Furukawa et al., since this would allow the formation of defined small-sized patterns (column 2, lines 47-50).

***Response to Arguments***

16. Applicant's arguments filed 4/30/2003 have been fully considered but they are not persuasive.

Applicants argue, "...claim 13, as well as claim 19, which depends on claim 13, recite that the pillars are coated with a low dielectric polymer. The Ping patent does not disclose or suggest the use of a low dielectric polymer...". In response to this argument, claim 13 teaches coating one or more pillars with a polymer coating, not coating "with a low dielectric polymer" as argued.

Also, in reference to claims 13 and 19, applicants argue, "...the Ping patent discloses the deposition of a silicon oxide layer and chemical mechanical processing (CMP) to avoid the off-gassing problem associated with the SOG. The invention on the other hand, simply uses a low dielectric polymer coating which totally eliminated the off-gassing problem and obviates the need for additional silicon dioxide layer...". In response to this argument, applicants assert that the Ping patent does not teach using low dielectric polymer coating, but neither does claims 13 and 19. Furthermore, the submitted prior art teaches using low dielectric polymer coating as part of the conventional process to reduce capacitive coupling and minimizing cross talk between adjacent metal layers.

Further still, applicants argue, "...neither the Lin or Kano patents disclose or suggest a process as recited in claims 1, 4 and 7...the Lin patent...teaches away from a plated pillars as recited in the claims at issue and instead discloses a pillar formed...solely from metal, unlike the invention recited in the claims at issue...the Kano

patent similarly fails to or suggest a plated pillar as recited in the claims at issue...". In response to this argument, Lin does not explicitly teach away from the invention. On the other hand, Kano does teach forming the plated pillars as taught by the prior art (Kano, column 5, lines 4 – 31, and Fig.2E).

***Conclusion***

17. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

18. Papers related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is **(703) 305-3432**. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Julio J. Maldonado** at **(703) 306-0098** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via julio.maldonado@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

JMR
7/11/03

George Fourson
Primary Examiner